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DERWENT-ACC-NO: 1992-133692
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TITLE: Thin film transistor with improved gate dielectric breakdown voltage - has thicker dielectric over angular and sidewall regions of gate electrode

INVENTOR: KIMURA, H; TSUTSUMI, K

PATENT-ASSIGNEE:

ASSIGNEE	CODE
MITSUBISHI DENKI KK	MITQ
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PRIORITY-DATA: 1991JP-0220277 (August 30, 1991), 1990JP-0274360 (October 12, 1990)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 6018181 A	January 25, 2000		000	H01L027/01
EP 481379 A	April 22, 1992	E	014	
DE 4134547 A	April 23, 1992		014	
JP 05029347 A	February 5, 1993		007	H01L021/336
DE 4134547 C2	January 20, 1994		014	H01L021/76
US 5378650 A	January 3, 1995		014	H01L021/76
EP 481379 B1	February 5, 1997	E	014	H01L029/772
DE 69124563 E	March 20, 1997		000	H01L029/772

DESIGNATED-STATES: DE FR NL DE FR NL

CITED-DOCUMENTS:3.Jnl.Ref; EP 102802 ; FR 2535528 ; JP 01229229 ; JP 61225869 ; JP 62048045 ; 5.Jnl.Ref ; JP 1229229

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
US 6018181A	October 11, 1991	1991US-0774103	CIP of
US 6018181A	March 1, 1993	1993US-0026111	Cont of
US 6018181A	December 16, 1994	1994US-0358050	
EP 481379A	October 11, 1991	1991EP-0117410	
DE 4134547A	October 18, 1991	1991DE-4034547	
JP 05029347A	August 30, 1991	1991JP-0220277	
DE 4134547C2	October 18, 1991	1991DE-4134547	
US 5378650A	October 21, 1991	1991US-0777711	Div ex
US 5378650A	January 21, 1993	1993US-0006394	
EP 481379B1	October 11, 1991	1991EP-0117410	
DE 69124563E	October 11, 1991	1991DE-0624563	
DE 69124563E	October 11, 1991	1991EP-0117410	
DE 69124563E		EP 481379	Based on

INT-CL (IPC): H01L 21/336; H01L 21/74; H01L 21/76; H01L 27/01; H01L 27/04; H01L 27/12; H01L 29/772; H01L 29/78; H01L 29/784

ABSTRACTED-PUB-NO: DE 4134547C
BASIC-ABSTRACT:

Thin film transistor comprises: gate electrode (1) formed on a insulating layer (10) and having opposite sidewalls; dielectric layer (3a, 3b) formed on the insulating layer and covering upper and side surfaces of the gate electrode with a thickness 5; semiconductor layer (8) on an upper surface of the dielectric with a channel region (2) formed above the gate electrode and a pair of impurity regions (4, 5) on opposite sides of the channel; an interface between dielectric and semiconductor lying in a single plane throughout a 1st region beneath channel and a 2nd region extending beyond each sidewall of the gate by a distance greater than thickness of dielectric t.

In a 2nd device a sidewall insulating layer is formed on the side surfaces of the gate and a dielectric layer on the surface of the gate, dielectric, and sidewall insulator. Mfg. devices includes: forming insulating layer (10); gate electrode (1); dielectric layers (3a, 3b) covering upper surface and side surface of gate and having a flat surface; semiconductor layer (8); impurity regions (4, 5) by forming a mask layer and ion implanting through it.

Dielectric layer consists of 1st layer (3a) over sidewall of gate with a thickness equal to that of the gate and a 2nd dielectric layer (3b) formed over the surface of 1st layer and having a flat surface. Dielectric layers are TEOS.

ADVANTAGE - Increased gate dielectric breakdown voltage by having dielectric thicker over the angular and sidewall regions of the gate electrode.
ABSTRACTED-PUB-NO:

EP 481379A
EQUIVALENT-ABSTRACTS:

The integrated circuit structure comprises semiconductor element regions (10) formed on a surface of a semiconductor substrate (10), surrounded by an isolating film (2a). First impurity regions (6) are formed by ion implantation under the film at a predetermined depth w.r.t. the interface between the film and the substrate. Simultaneously, second impurity regions are formed in the semiconductor element regions at a predetermined depth, spatially arranged to prevent punch-through of field effect transistors formed in the semiconductor element regions. A sidewall insulation film (8a) is formed at the vertical walls of the film (2a).

ADVANTAGE - Enables increased miniaturisation.

EP 481379B

A thin film transistor, comprising gate electrode (1) formed on an insulating layer (10) and having opposite sidewalls; a dielectric layer (3a,3b) formed on the insulating layer (10) and covering upper and side surfaces of the gate electrode (1), the dielectric layer (3b) overlying the gate electrode (1) having a flat surface and a thickness t, and a semiconductor layer (8) formed on an upper surface of the dielectric layer (3a,3b), an interface between the dielectric layer (3a,3b) and the semiconductor layer (8) lying in a single plane throughout a first region above the gate electrode (1) and a second region extending beyond each the sidewall of the gate electrode (1) by a distance greater than the thickness t of the dielectric layer (3b), characterised in that the semiconductor layer (8) has a channel region (2) formed above the gate electrode (1) and has a pair of impurity regions (4,5) formed respectively at opposite sides of the channel region (2), the dielectric layer (3a,3b) comprises a first insulating layer (3a) formed in contact with the sidewall of the gate electrode (1) and having a film thickness equal to that of the gate electrode (1) and a second insulating layer (3b) formed on the surface of this first insulating layer (3a).

US 5378650A

The semiconductor device is mfd. by (a) forming a 1st insulator film on a semiconductor substrate, (b) patterning to form an isolating insulator film with a vertical sidewall, (c) ion implantation to form a 1st impurity region between the insulator film and substrate, and to form 2nd impurity regions sepd. by the film and used to form a semiconductor circuit element, the 2nd impurity regions being located to prevent punch-through of the circuit elements, (d) forming a 2nd insulator film to cover the isolating insulator film and main surface of the substrate, and (e) anisotropic etching the 2nd insulator film to leave a sidewall insulator film on the vertical sidewall of the isolating insulator film.

ADVANTAGE - Increased integration without a deterioration in performance.

US 6018181A

Thin film transistor comprises: gate electrode (1) formed on a insulating layer (10) and having opposite sidewalls; dielectric layer (3a, 3b) formed on the insulating layer and covering upper and side surfaces of the gate electrode with a thickness 5; semiconductor layer (8) on an upper surface of the dielectric with a channel region (2) formed above the gate electrode and a pair of impurity regions (4, 5) on opposite sides of the channel; an interface between dielectric and semiconductor lying in a single plane throughout a 1st region beneath channel and a 2nd region extending beyond each sidewall of the gate by a distance greater than thickness of dielectric t.

In a 2nd device a sidewall insulating layer is formed on the side surfaces of the gate and a dielectric layer on the surface of the gate, dielectric, and sidewall insulator. Mfg. devices includes: forming insulating layer (10); gate electrode (1); dielectric layers (3a, 3b) covering upper surface and side surface of gate and having a flat surface; semiconductor layer (8); impurity regions (4, 5) by forming a mask layer and ion implanting through it.

Dielectric layer consists of 1st layer (3a) over sidewall of gate with a thickness equal to that of the gate and a 2nd dielectric layer (3b) formed over the surface of 1st layer and having a flat surface. Dielectric layers are TEOS.

ADVANTAGE - Increased gate dielectric breakdown voltage by having dielectric thicker over the angular and sidewall regions of the gate electrode.

CHOSEN-DRAWING: Dwg.2B/5 Dwg.7/9 Dwg.1/9 Dwg.1/5

TITLE-TERMS: THIN FILM TRANSISTOR IMPROVE GATE DIELECTRIC BREAKDOWN VOLTAGE THICK DIELECTRIC ANGULAR SIDEWALL REGION GATE ELECTRODE

DERWENT-CLASS: L03 U11 U12

EPI-CODES: U11-C18A1; U12-B03A; U12-D02A;

SECONDARY-ACC-NO:
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